Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -o C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter\_tb\_isim\_beh.exe -prj C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter\_tb\_beh.prj work.nbit\_twisted\_ring\_counter\_tb

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/D\_flipflop.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_reg.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/not\_gate.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_shiftreg.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter\_tb.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package std\_logic\_arith

Compiling package std\_logic\_unsigned

Compiling architecture behavioral of entity not\_gate [not\_gate\_default]

Compiling architecture behavioral of entity D\_flipflop [d\_flipflop\_default]

Compiling architecture behavioral of entity nbit\_reg [\nbit\_reg(8)\]

Compiling architecture behavioral of entity nbit\_shiftreg [\nbit\_shiftreg(8)\]

Compiling architecture behavioral of entity nbit\_twisted\_ring\_counter [\nbit\_twisted\_ring\_counter(8)\]

Compiling architecture behavior of entity nbit\_twisted\_ring\_counter\_tb

Time Resolution for simulation is 1ps.

Waiting for 2 sub-compilation(s) to finish...

Compiled 15 VHDL Units

Built simulation executable C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter\_tb\_isim\_beh.exe

Fuse Memory Usage: 33104 KB

Fuse CPU Usage: 529 ms